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For: ELECTRON BEAM PROJECTION MASK

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VERIFICATION OF TRANSLATION

Dear Sir:

The undersigned hereby certifies that I am conversant in both the Japanese and English languages, that I have prepared the attached English translation of the Japanese priority Application (Japanese Application No. 2001-016085 filed January 24, 2001), attached as **Exhibit A**, and that the English translation is a true, faithful and accurate translation of the attached **Exhibit A**.

I further declare that all statements made of my own knowledge are true and that all statements made on information and belief are with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC § 1001, and that such false statements may jeopardize the validity of the application or any patent issuing therefrom.

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[Document Title] Specification

[Title of the Invention] Electron Beam Projection Mask

[What Is Claimed Is]

[Claim 1] An electron beam projection mask for arranging a plurality of batch projection regions so that a pattern density may be equalized all over a surface of a semiconductor substrate.

[Claim 2] An electron beam projection mask according to claim 1, wherein the mask is a stencil type mask.

[Claim 3] An electron beam projection mask according to claim 1, wherein the mask is a membrane type mask.

[Claim 4] An electron beam projection mask according to any one of claims 1 to 3, wherein the mask is a partial batch electron beam exposure mask.

[Claim 5] An electron beam projection mask as claimed in any one of claims 1 to 3, wherein the mask is an electron beam projection lithography mask.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The Present invention relates to an electron beam projection mask, and particularly, to an electron beam projection mask (electron-beam(EB) exposure mask) for

arranging a plurality of batch projection regions on the whole wafer surface.

[0002]

[Prior Art]

In recent years, in accordance with a development of a high-density integrated circuit, an ultra-microfabrication technology is required for forming semiconductor elements and wiring which form an integrated circuit, and there is a demand for developing a technique for realizing it.

[0003]

For example, in order to form a fine pattern having a line with 0.1 μm or less width, there is a technology using an electron beam to perform fine patterning when a resist film is exposed.

[0004]

Since the electron beam has a very short wavelength as a matter-wave as compared with a wavelength used in other exposure technologies, and its diffraction aberration is so small that it can be disregarded, the electron beam exposure essentially has a high resolution. However, in the electron beam exposure technique (EB direct drawing), since a pattern is drawn by a rectangle shape electron beam with a size of about several μm, there is a disadvantage

that a throughput is low. This method is called a variable-shaped electron beam exposure method.

[0005]

In order to improve the low throughput, at present, a technology of a partial batch electron beam exposure (also called as a cell projection or a block exposure) is practically used. This partial batch electron beam exposure technology is described, for example, in the Japanese Patent Laid-Open No.7-161605.

[0006]

This partial batch electron beam exposure technology is for projecting a pattern of several squire μm area at once which appears repeatedly in a device pattern, by using a stencil type electron beam mask (also called as Si stencil mask, an aperture, a partial batch mask, a cell projection mask, or a block mask) having an opening in Si film with about 20 μm thickness. Accordingly, the number of shots of the electron beam is greatly reduced compared to the conventional EB direct drawing technology, and an improvement in throughput can be attained.

[0007]

However, even if this partial batch electron beam exposure method is used, for a pattern without the repetition in the device patterns, the pattern must be

directly drawn by the electron beam of the rectangle shape with a size of about several squire μm (variable-shaped electron beam exposure method). For this reason, a further improvement in the throughput is required for mass-production.

[0008]

An electron beam exposure method which aims at an extremely high throughput compared to the partial batch electron beam exposure method is proposed in recent years. That is an electron beam reduction projection apparatus using a mask having a whole circuit pattern of a semiconductor chip, irradiates an electron beam to some region of the mask, thus the reduction pattern of the region passes a projection lens and forms an image of the pattern. Generally, this technology is called an electron beam projection lithography (abbreviated as EPL). This EPL technology is described in the Japanese Patent Laid-Open No.2000-58446, for example.

[0009]

Conventionally, the region which can be projected at once by the variable-shaped electron beam exposure method or partial batch exposure method was as small as 5 square μm.

However, with the above-mentioned EPL technology, the

region which can be projected at once is quite large with 250 squareμm, thereby the throughput is improved greatly.

[0010]

Although a mask is used for the above-mentioned partial batch electron beam exposure technology and EPL technology, the nonpermissible curvature or distortion of the mask arise at the time of manufacturing the mask and irradiating the electron beam, and there is a problem that the position accuracy of a pattern deteriorates.

[0011]

Fig. 4 shows a schematic figure of the conventional EPL (electron beam projection lithography) mask.

[0012]

When a pattern intended to be drawn is prepared, it generally has a pattern density which is not uniform and is out of balance, as shown in Fig 4(a). Here, assuming that the region 41 (diagonal region) with a high pattern density and the region 42 (white region) with a low pattern density spread as shown in Fig. 4 (a).

[0013]

Next, when the size of a batch projection region on a mask is 1mm , the drawing pattern is divided into the size of 1mm as shown in Fig. 4(b).

[0014]

Finally, when arranging 1mm size batch projection regions on an 8 inches silicon wafer 43, as shown in Fig. 4(c), they are usually so arranged that the move distance, i.e., the move time, from a certain batch projection region to the next batch projection region becomes shorter. Therefore, in many cases, the batch projection regions are arranged so that the adjacency relations of the original drawing pattern may not be changed as much as possible.

[0015]

Consequently, the imbalance of the pattern density arises all over the 8 inches wafer, and stress occurs in concentration at the imbalance parts at the time of mask manufacturing and electron beam irradiation, thus curvature and distortion arise on the wafer. Accordingly, the position accuracy of the pattern worsen.

[0016]

In the EPL mask, it is one of the important elements to provide high projection accuracy.

[0017]

As a technology relevant to the present invention, there is a technology described in the Japanese Patent Laid-Open No. 7-66098.

[0018]

[Problems to be Solved by the Invention]

However, in the conventional mask manufacturing method, there were problems that the imbalance of the pattern density arose all over the wafer, the stress generated at the time of mask manufacturing and electron beam irradiation is concentrated on the imbalance portion, the curvature and distortion of a wafer arose, and the position accuracy of a pattern deteriorated.

[0019]

For example, in the Japanese Patent Laid-Open No. 63-110634, a manufacturing method of the mask for X-ray steppers is described. In this publication, it is disclosed that since the X-ray stepper uses an X-ray absorbing material having same density for a pattern region and a cover region, shrinkage and curvature of the absorbing material by the stress are prevented.

[0020]

This technology is effective in some degree to relieve the stress in a single batch projection region.

[0021]

However, in this invention, in the case of a mask with which a plurality of batch projection regions are arranged in manner of a matrix, an equalization of the pattern density on the whole wafer surface isn't realized. Rather, there is a possibility of enlarging imbalance of

the pattern density on the whole wafer surface, and the stress concentrated on the specific region of the whole wafer surface cannot be prevented.

[0022]

[Means for Solving the Problems]

The electron beam projection mask of the present invention is characterized by arranging batch projection regions in such a manner that the pattern density is to be equalized on the whole semiconductor substrate surface.

[0023]

[Embodiments of the Invention]

Fig. 1 shows a schematic view of an embodiment of the electron beam projection mask according to the present invention.

[0024]

When arranging batch projection regions having a predetermined size in the manner of matrix (12) on the 8 inches wafer 11 used as a semiconductor substrate, they are so arranged that the pattern density may be equalized as much as possible on the whole wafer surface.

[0025]

For example, the region 14 (diagonal region) where pattern density is high and the region 13 (white region) where pattern density is low are alternatively arranged

like a checkered flag.

[0026]

When they are arranged in this way, the imbalance of the pattern density on the whole 8 inches wafer surface decreases, thus a stress generated at the time of mask manufacturing and electron beam irradiation decreases. As a result, the curvature and distortion of the wafer become small, and degradation of the position accuracy of the pattern can be prevented.

[0027]

[Embodiment]

The embodiment of the present invention is hereafter explained in detail using drawings.

[0028]

Fig. 2 shows a schematic diagram of the EPL (electron beam projection lithography) mask as one embodiment of the present invention.

[0029]

First, a pattern intended to be drawn has, when prepared, a pattern density which is not uniform and is out of balance all over the substrate, as shown in Fig. 2(a).

[0030]

Here, the region 21 (diagonal region) where pattern density is high and the region 22 (white region) where

pattern density is low are distributed, as shown in Fig. 2(a), respectively.

[0031]

Next, if the size of the batch projection region on a mask is 1mm , a drawing pattern is divided into 1mm portions as shown in Fig. 2(b).

[0032]

Finally, when arranging the batch projection regions of 1mm on the 8 inches silicon wafer 23 used as a semiconductor substrate, the batch projection regions are arranged, for example, in the manner of a checkered flag so that the pattern density may be equalized as much as possible on the whole wafer surface, as shown in Fig. 2(c).

[0033]

Thus, when the imbalance of the pattern density on the whole 8 inches wafer surface decreases, a stress generated at the time of mask manufacturing and electron beam irradiation decreases, so that the curvature and distortion of a mask and wafer become small, and deterioration of the position accuracy of a pattern can be prevented.

[0034]

Moreover, as shown in Fig. 3, pattern density can also be equalized by arranging the batch projection regions

so that the region 31 (diagonal region) where pattern density is high and the region 32 (white region) where pattern density is low form a stripe shape, alternatively.

[0035]

In the above-mentioned embodiment, although the present invention is applied to an EPL (electron beam projection lithography) mask, the same effect can be achieved when it is applied to a partial batch electron beam exposure mask.

[0036]

Here, an electron beam (EB for short) exposure mask is explained.

[0037]

Conventionally, in the electron beam exposure method, the pattern is drawn in a manner of single stroke, without using a mask at all. In this method, since a mask is not necessary, it does not cost for a mask. Moreover, there is an advantage that, for example, it does not need to re-create a mask from a sketch to change some mask patterns suddenly.

[0038]

However, the EB exposure method has a low throughput which prevents mass-production.

[0039]

Recently, a mask is also used for the electron beam exposure to improve the throughput. The mask used for the EB exposure method may be a stencil type mask and a membrane type mask, broadly.

[0040]

A stencil mask and its production method are described in, for example, the Japanese Patent Laid-Open No. 5-216216. The stencil mask has an opening (does not have any substance), and electrons are pass through the opening, but at a portion without an opening, electrons are scattered and does not pass through. Usually, the opening pattern is formed by dry etching which uses chemical gas to make a hole on the silicon wafer. The stencil type mask is advantageous to earn an excellent contrast. An electron passes through the opening without being scattered since the opening does not have a substance. In contrast, since the portion without the opening has a predetermined thickness of silicon, almost all electrons can not pass (mere a few passes). However, since a pattern is formed by an opening, a doughnut pattern or the like can not be realized because an inner pattern falls.

[0041]

On the other hand, a membrane type mask is described in the Japanese Patent Laid-Open No. 5-62888. The membrane

type mask is made by forming an electron dispersion film on an electron penetration film, and patterning only the electron dispersion film. The portion in which the electron dispersion film remains does not let an electron pass, but the portion in which an electron dispersion film does not exist (namely, portion in which only an electron penetration film exists) makes an electron penetrate.

[0042]

However, even the electron penetration film is used, since some electrons are scattered, the contrast is not so excellent as the stencil type mask. However, since the electron dispersion film has been arranged on the electron penetration film, a doughnut pattern can be formed.

[0043]

Though this membrane type mask has been developed for X-ray lithography, it is also possible to use for EB lithography, so it is used for EB lithography at present. That is, many of membrane type masks used for X-ray lithography can be also used for electron lithography. Fundamentally, the X-ray dispersion body scatters electrons, and an X-ray penetration body allows electrons to penetrate. Generally, the mask is produced by using a silicon nitride film as an electron penetration body, and covered with heavy metals such as tungsten and chromium as an electron

dispersion body.

[0044]

In addition, in the industry of EB lithography, the mask means the stencil type mask in many cases. Also the mask is called as an aperture or a reticle. It is because the mask having openings is advantageous in order to improve contrast.

[0045]

However, in recent years, there is a technology of EPL which enables a batch exposure of the large area to realize a high throughput. This technology aims to carry out the batch exposure of the large area, and a doughnut pattern is also concerned. Therefore, there is a movement to apply the membrane type mask which can also form a doughnut pattern. Even in the case of stencil type mask, if a doughnut pattern is divided into two masks and perform a projection exposure with the two masks, a doughnut pattern can be formed.

[0046]

[Effects of the Invention]

According to the present invention, as explained above, when the imbalance of the pattern density on the whole wafer surface decreases, stress generated at the time of mask manufacturing and electron beam irradiation

decreases, the curvature and distortion of a wafer become small, thus deterioration of the position accuracy of a pattern can be prevented.

[Brief Description of the Drawings]

Fig. 1 is a schematic diagram showing an embodiment of the electron beam projection mask of the present invention;

Fig. 2 is a schematic diagram showing an EPL (electron beam projection lithography) mask of an embodiment of the present invention;

Fig. 3 is a schematic diagram showing an EPL mask of another embodiment of the present invention; and

Fig. 4 is a schematic diagram showing a conventional EPL mask.

[Description of the Reference Numerals]

11 wafer

12 batch projection region arranged in matrix shape

14 region with high pattern density

13 region with low patter density

21, 31 region with high pattern density

22, 32 region with low patter density

23, 33 silicon wafer

[Document Title] Abstract

[Abstract]

[Object] To prevent degrading of a positioning accuracy of a pattern by reducing curvature and distortion of a wafer.

[Scheme] Batch projection regions 13, 14 of an electron beam projection mask are arranged so that the pattern density may be equalized on the whole wafer surface.

[Selected Drawing] Fig. 1